Dual 5-A High-Speed Low-Side Gate Driver Based on CMOS Input Threshold Logic

Check for Samples: UCC27527, UCC27528

FEATURES

- **Industry-Standard Pin Out**
- **Two Independent Gate-Drive Channels**
- **5-A Peak Source and Sink Drive Current**
- **CMOS Input Logic Threshold (function of supply voltage on VDD pins)**
- **Hysteretic Logic Thresholds for High Noise Immunity**
- **Independent Enable Function for Each Output**
- **Inputs and Enable Pin Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage**
- **4.5-V to 18-V Single Supply Range**
- **Outputs Held Low During VDD UVLO, (ensures glitch-free operation at power-up and power-down)**
- **Fast Propagation Delays (17-ns typical)**
- **Fast Rise and Fall Times (7-ns and 6-ns typical)**
- **1-ns Typical Delay Matching Between 2-Channels**
- **Outputs Held in LOW When Inputs Floating**
- **SOIC-8, and 3-mm x 3-mm WSON-8 Package Options**
- **Operating Temperature Range of -40°C to 140°C**
- **-5-V Negative Voltage Handling Capability on Input and Enable Pins**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC-to-DC Converters**
- **Motor Control, Solar Power**
- **Gate Drive for Emerging Wide Band Gap Power Devices such as GaN**

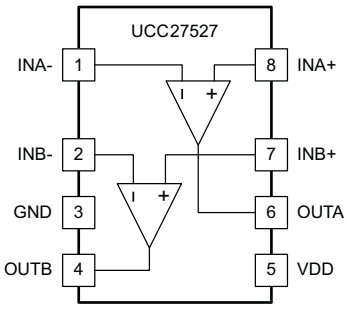
DESCRIPTION

The UCC2752x family of devices are dual-channel, high-speed, low-side gate driver devices capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC2752x is capable of delivering high-peak current pulses of up to 5-A source and 5-A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay typically 17 ns. In addition, the drivers feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. The input pin thresholds are based on CMOS logic, which is a function of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity. The Enable pins are based on TTL and CMOS compatible logic, independent of VDD supply voltage.

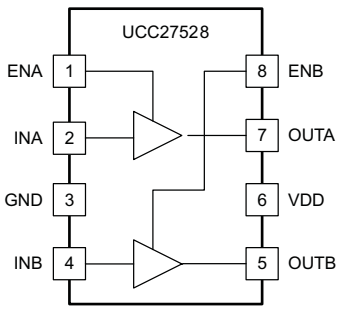
PRODUCT PREVIEW

Product Matrix

Dual Input Configuration



Dual Non-Inverting Inputs



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONT.)

The UCC27528 is a dual non-inverting driver. UCC27527 features a dual input design which offers flexibility of both inverting (IN- pin) and non-inverting (IN+ pin) configuration for each channel. Either IN+ or IN- pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For safety purpose, internal pull-up and Pull-down resistors on the input pins of all the devices in UCC2752x family in order to ensure that outputs are held LOW when input pins are in floating condition. UCC27528 features Enable pins (ENA and ENB) to have better control of the operation of the driver applications. The pins are internally pulled up to VDD for active high logic and can be left open for standard operation.

ORDERING INFORMATION(1)(2)

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE, T_A
UCC27527	SOIC 8-Pin (D) and WSON 8-pin (DSD)	-40°C to 140°C
UCC27528	SOIC 8-Pin (D) and WSON 8-pin (DSD)	

(1) For the most current package and ordering information, see Package Option Addendum at the end of this document.
(2) All packages use Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations. DSD package is rated MSL level 2.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3 to	20.0	V
OUTA, OUTB voltage	DC	-0.3 to	VDD + 0.3	V
	Repetitive pulse < 200 ns(3)	-2.0 to	VDD + 0.3	V
Output continuous source/sink current	I_{OUT_DC}		0.3	A
Output pulsed source/sink current (0.5 µs)	I_{OUT_pulsed}		5	A
INA, INB, INA+, INA-, INB+, INB-, ENA, ENB voltage(4)		-6.5	20	V
ESD(5)	Human body model, HBM		4000	V
	Charge device model, CDM		1000	V
Operating virtual junction temperature, T_J range		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) Values are verified by characterization on bench.
(4) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the VDD pin.
(5) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	-40		140	°C
Input voltage, INA, INB, INA+, INA-, INB+, INB-	-5		18	V
Enable voltage, ENA and ENB	-5		18	

THERMAL INFORMATION

THERMAL METRIC		UCC27527, UCC27528		UNITS
		D	DSD	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	128	46.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	77.7	50.7	
θ_{JB}	Junction-to-board thermal resistance(3)	68.5	21.8	
ψ_{JT}	Junction-to-top characterization parameter(4)	20.7	1.1	
ψ_{JB}	Junction-to-board characterization parameter(5)	68.0	22.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	n/a	9.0	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, T_A = T_J = -40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Bias Currents						
$I_{DD(off)}$	Startup current, (based on UCC27524 Input configuration)	VDD = 3.4 V, INA=VDD, INB=VDD	55	125	225	µA
		VDD = 3.4 V, INA=GND, INB=GND	25	125	225	
Under Voltage LockOut (UVLO)						
V_{ON}	Supply start threshold	T_J = 25°C	3.91	4.20	4.50	V
		T_J = -40°C to 140°C	3.75	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start		3.60	3.90	4.40	
VDD_H	Supply voltage hysteresis		0.20	0.30	0.50	
Inputs (INA, INB, INA+, INA-, INB+, INB-), UCC2752X (D, DSD)						
V_{IN_H}	Input signal high threshold	Output high for non-inverting input pins Output low for inverting input pins		55	70	%V_{DD}
V_{IN_L}	Input signal low threshold	Output low for non-inverting input pins Output high for inverting input pins	30	38		
V_{IN_HYS}	Input hysteresis			17		
Enable (ENA, ENB) UCC2752X (D, DSD)						
V_{EN_H}	Enable signal high threshold	Output enabled	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output disabled	0.95	1.10	1.25	
V_{EN_HYS}	Enable hysteresis		0.70	0.80	1.10	
Outputs (OUTA, OUTB)						
$I_{SNK/SRC}$	Sink/source peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
V_{DD}-V_{OH}	High output voltage	I_{OUT} = -10 mA			0.075	V
V_{OL}	Low output voltage	I_{OUT} = 10 mA			0.01	
R_{OH}	Output pull-up resistance(2)	I_{OUT} = -10 mA	2.5	5	7.5	Ω
R_{OL}	Output pull-down resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω
Switching Time						
t_R	Rise time (3)	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		7		ns
t_F	Fall time(3)	C_{LOAD} = 1.8 nF, V_{DD} = 10 V		6		
t_M	Delay matching between 2 channels	INA = INB, OUTA and OUTB at 50% transition point, V_{DD} = 10 V		1	4	
t_{PW}	Minimum input pulse width that changes the output state(3)	V_{DD} = 10 V		15		
t_{D1}, t_{D2}	Input to output propagation delay (3)	C_{LOAD} = 1.8 nF, 7-V input pulse, V_{DD} = 10 V	6	17	26	
t_{D3}, t_{D4}	EN to output propagation delay (3)	C_{LOAD} = 1.8 nF, 7-V enable pulse, V_{DD} = 10 V	6	13	23	

(1) Ensured by design.
(2) R_{OH} represents on-resistance of only the P-Channel MOSFET device in pull-up structure of UCC2752X output stage.
(3) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4

PRODUCT PREVIEW

Timing Diagrams

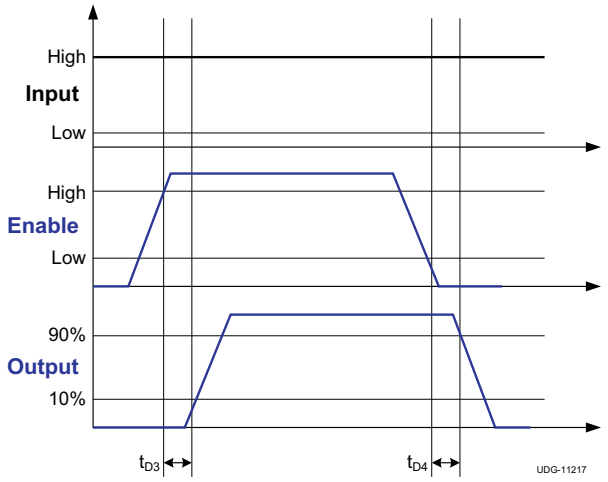

Figure 1. Enable Function (for non-inverting input driver operation)

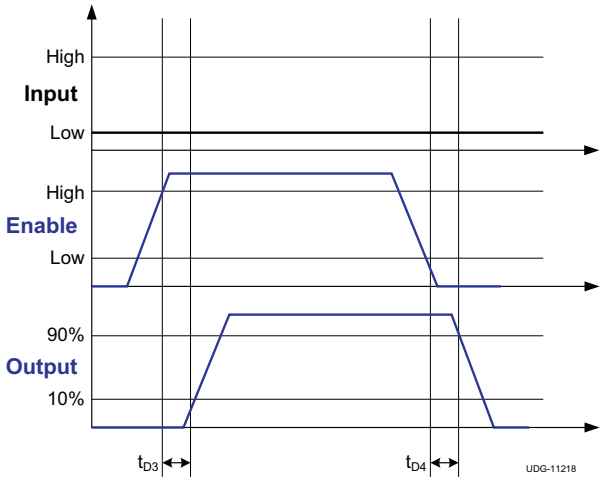

Figure 2. Enable Function (for inverting input driver operation)

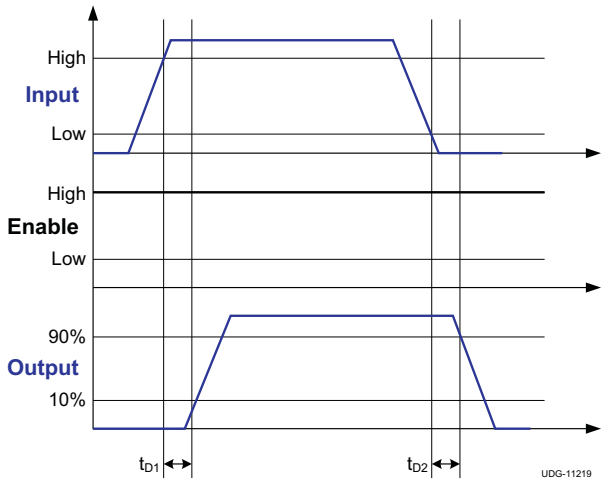

Figure 3. Non-Inverting Input Driver Operation

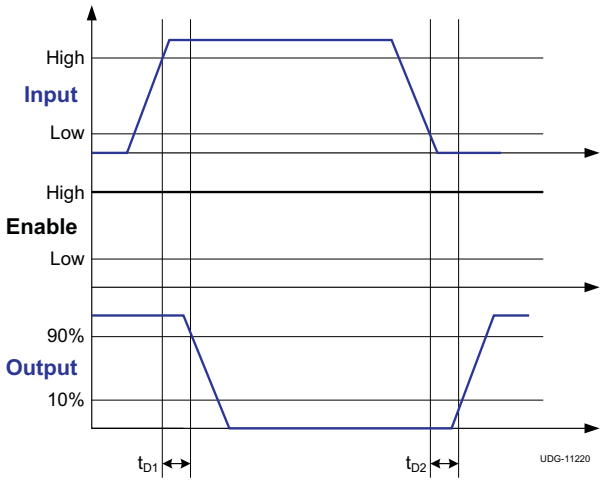

Figure 4. Inverting Input Driver Operation

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DEVICE INFORMATION

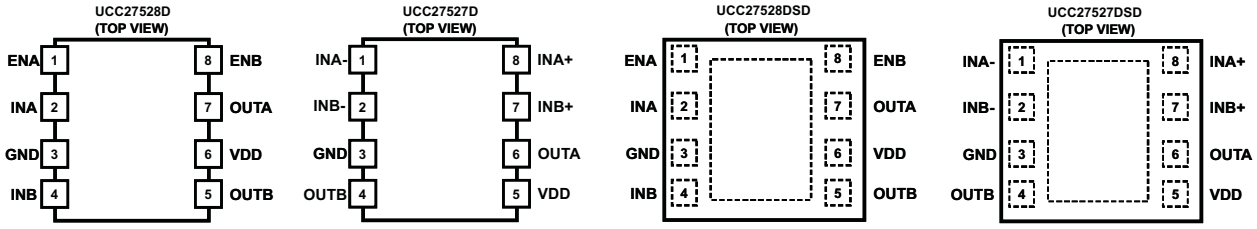

Figure 5.

TERMINAL FUNCTIONS (UCC27527)

TERMINAL		I/O	FUNCTION
NUMBER	NAME		
1	INA-	I	**Inverting Input to Channel A:** when Channel A is used in Non-Inverting configuration connect INA- to GND in order to Enable Channel A output, OUTA held LOW if INA- is unbiased or floating.
2	INB-	I	**Inverting Input to Channel B:** when Channel B is used in Non-Inverting configuration connect INB- to GND in order to Enable Channel B output, OUTB held LOW if INB- is unbiased or floating.
3	GND	-	**Ground:** All signals referenced to this pin.
4	OUTB	I	**Output of Channel B**
5	VDD	O	**Bias Supply Input**
6	OUTA	I	**Output of Channel A**
7	INB+	O	**Non-Inverting Input to Channel B:** When Channel B is used in Inverting configuration connect INB+ to VDD in order to Enable Channel B output, OUTB held LOW if INB+ is unbiased or floating.
8	INA+	I	**Non-Inverting Input to Channel A:** When Channel A is used in Inverting configuration connect INA+ to VDD in order to Enable Channel A output, OUTA held LOW if INA+ is unbiased or floating.

TERMINAL FUNCTIONS (UCC27528)

TERMINAL		I/O	FUNCTION
NUMBER	NAME		
1	ENA	I	**Enable input for Channel A:** ENA biased LOW Disables Channel A output regardless of INA state, ENA biased HIGH or floating Enables Channel A output, ENA allowed to float.
2	INA	I	**Input to Channel A:** Non-Inverting Input in UCC27528, OUTA held LOW if INA is unbiased or floating.
3	GND	-	**Ground:** All signals referenced to this pin.
4	INB	I	**Input to Channel B:** Non-Inverting Input in UCC27528, OUTB held LOW if INB is unbiased or floating.
5	OUTB	O	**Output of Channel B**
6	VDD	I	**Bias supply input**
7	OUTA	O	**Output of Channel A**
8	ENB	I	**Enable input for Channel B:** ENB biased LOW Disables Channel B output regardless of INB state, ENB biased HIGH or floating Enables Channel B output, ENB allowed to float.

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Table 1. Device Logic Table (UCC27528)

				UCC27528	
ENA	**ENB**	**INA**	**INB**	**OUTA**	**OUTB**
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition.

Table 2. Device Logic Table (UCC27527)

INx+ (x = A or B)	INx- (x = A or B)	OUTx (x = A or B)
L	L	L
L	H	L
H	L	H
H	H	L
x(1)	Any	L
Any	x(1)	L

(1) x = Floating condition.

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PRODUCT PREVIEW

Functional Block Diagrams

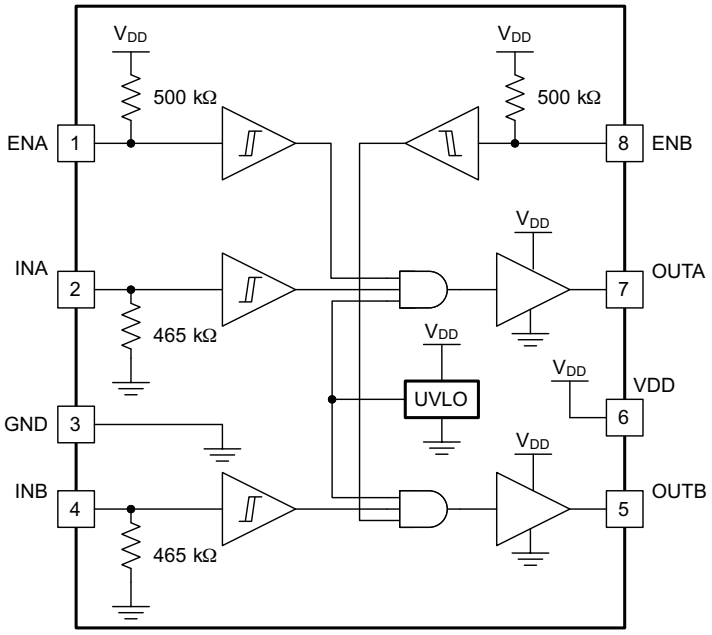

Figure 6. UCC27524 Block Diagram

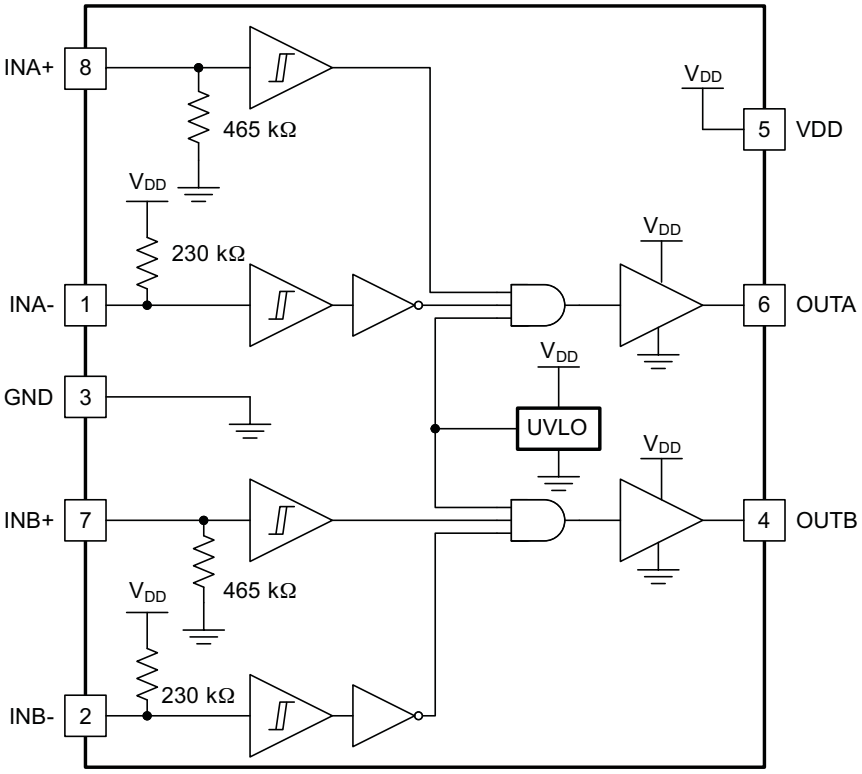

Figure 7. UCC27527 Block Diagram

TYPICAL CHARACTERISTICS

START-UP CURRENT vs TEMPERATURE

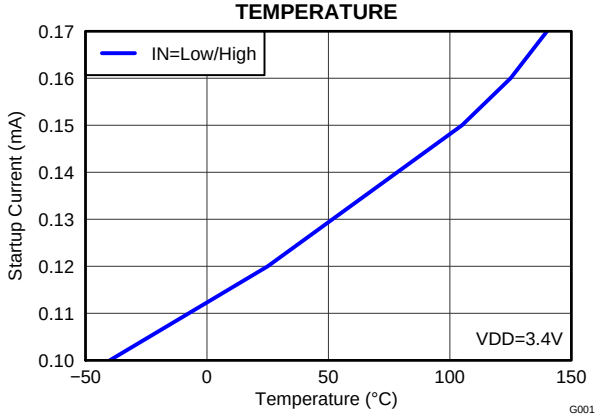

Figure 8.

OPERATING SUPPLY CURRENT vs TEMPERATURE (Outputs switching)

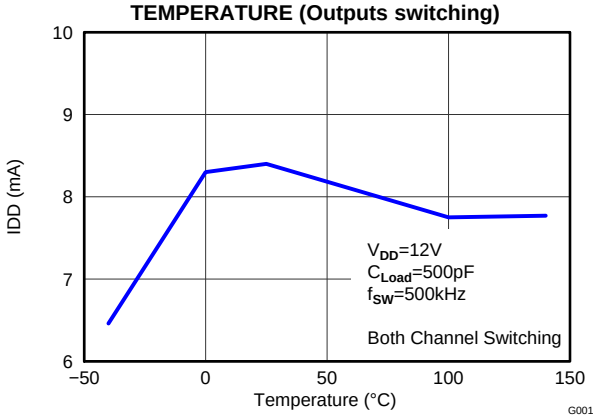

Figure 9.

SUPPLY CURRENT vs TEMPERATURE (Outputs in DC on/off condition)

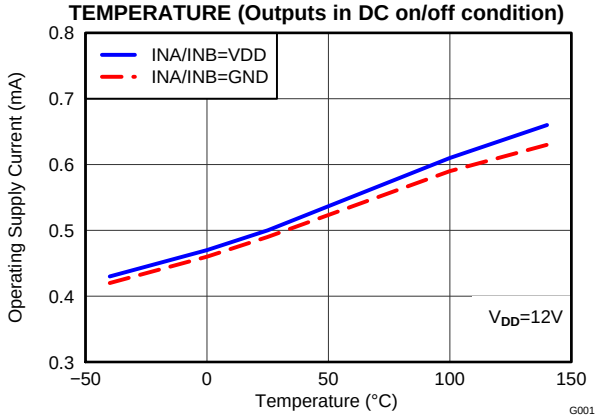

Figure 10.

UVLO THRESHOLD vs TEMPERATURE

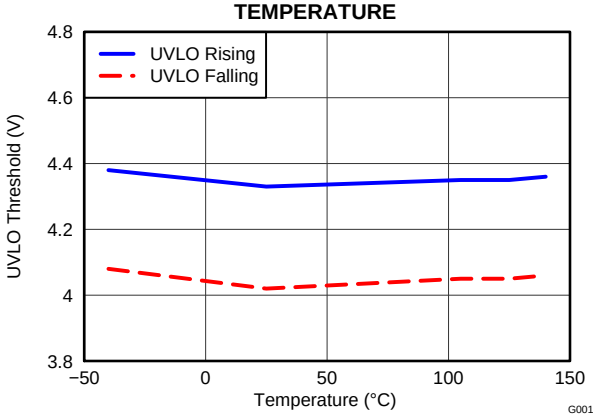

Figure 11.

INPUT THRESHOLD vs TEMPERATURE

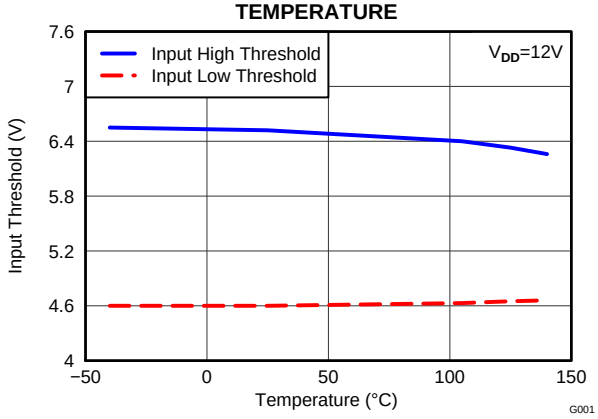

Figure 12.

ENABLE THRESHOLD vs TEMPERATURE

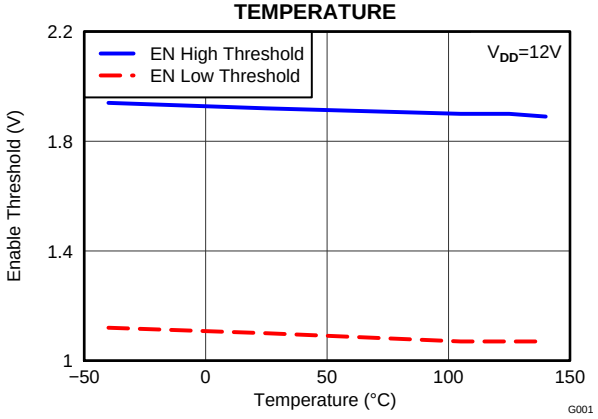

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

OUTPUT PULL-UP RESISTANCE vs TEMPERATURE

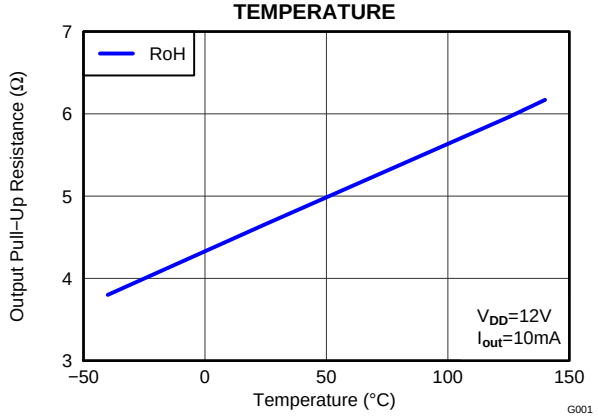

Figure 14.

OUTPUT PULL-DOWN RESISTANCE vs TEMPERATURE

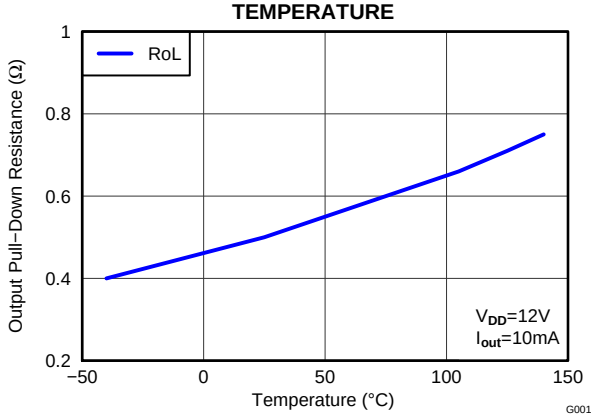

Figure 15.

RISE TIME vs TEMPERATURE

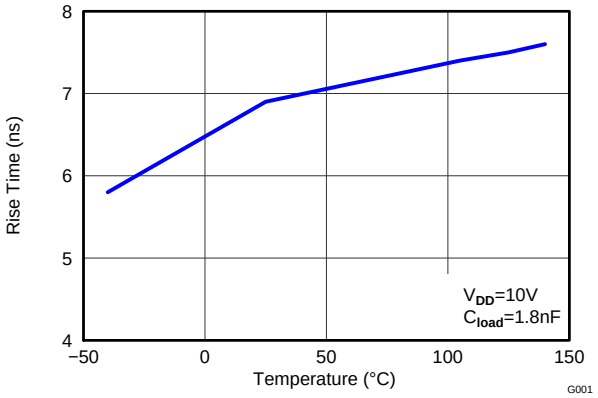

Figure 16.

FALL TIME vs TEMPERATURE

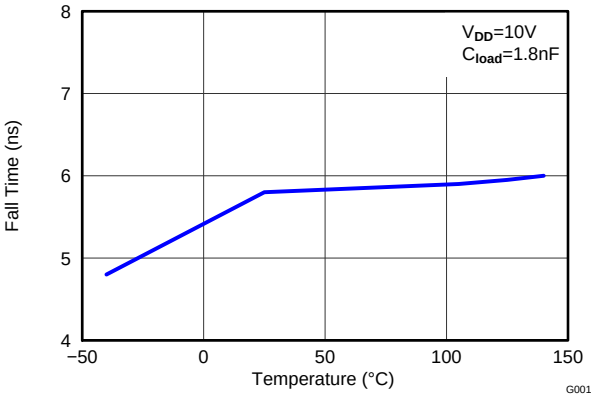

Figure 17.

INPUT TO OUTPUT PROPAGATION DELAY vs TEMPERATURE

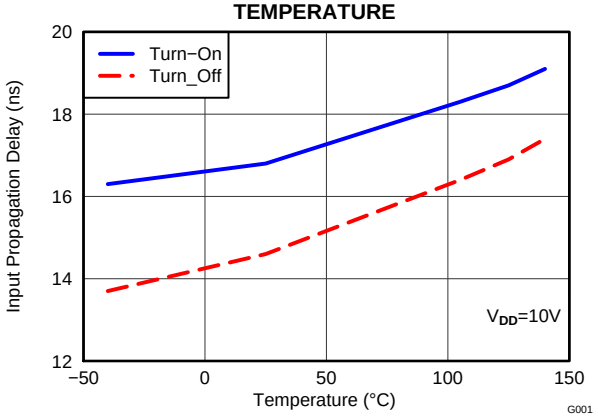

Figure 18.

EN TO OUTPUT PROPAGATION DELAY vs TEMPERATURE

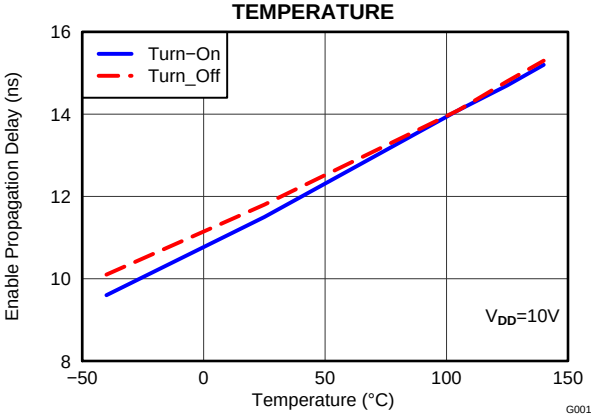

Figure 19.

TYPICAL CHARACTERISTICS (continued)

OPERATING SUPPLY CURRENT vs FREQUENCY

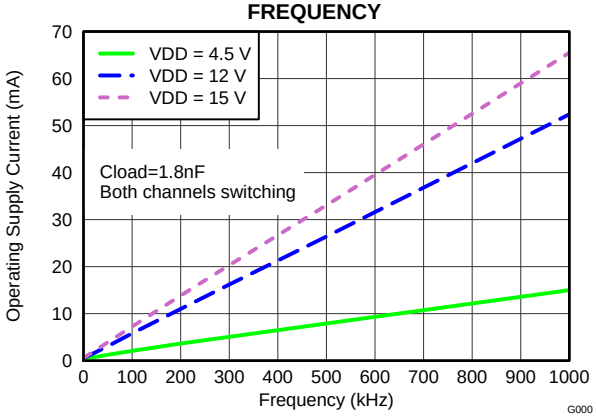

Figure 20.

PROPAGATION DELAYS vs SUPPLY VOLTAGE

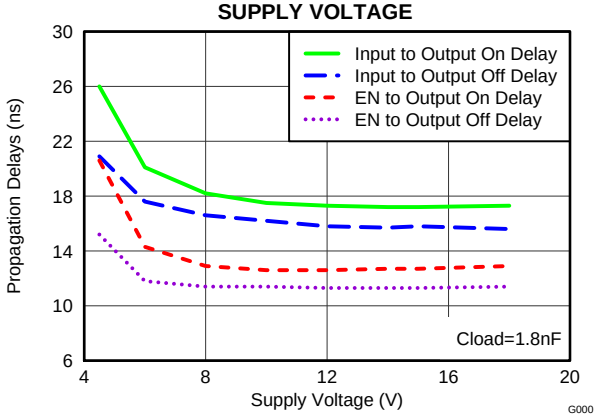

Figure 21.

RISE TIME vs SUPPLY VOLTAGE

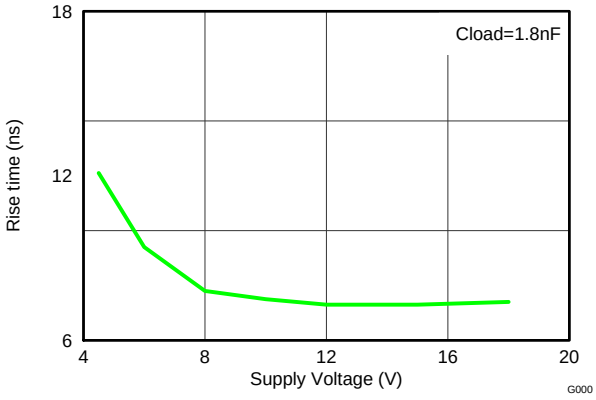

Figure 22.

FALL TIME vs SUPPLY VOLTAGE

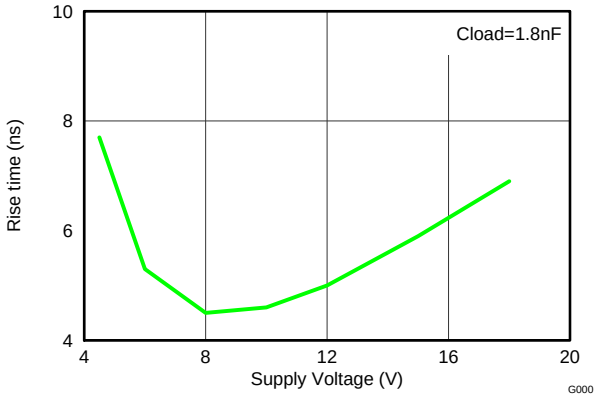

Figure 23.

ENABLE THRESHOLD vs TEMPERATURE

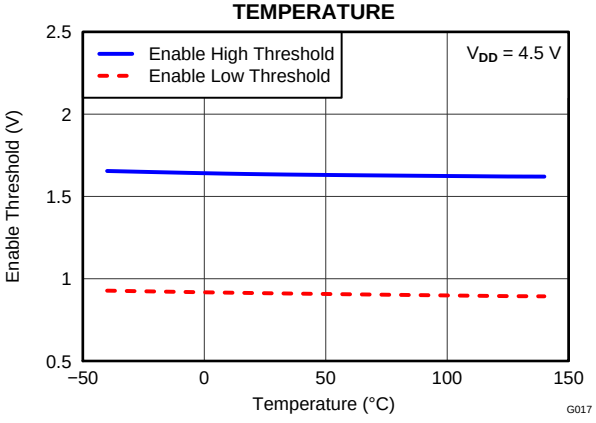

Figure 24.

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APPLICATION INFORMATION

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver device can be employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when sometimes it is just not feasible to have the PWM controller device directly drive the gates of the switching devices. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer drive functions. Gate driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate charge power losses into itself. In summary Gate-driver devices are an extremely important component in switching power combining benefits of high performance, low cost, component count, board-space reduction and simplified system design.

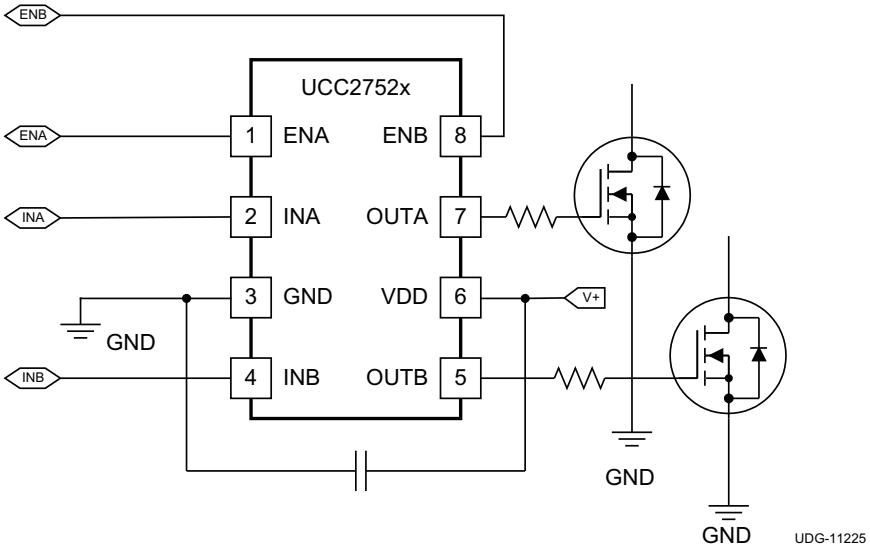

Figure 25. UCC2752x Typical Application Diagram (x = 8)

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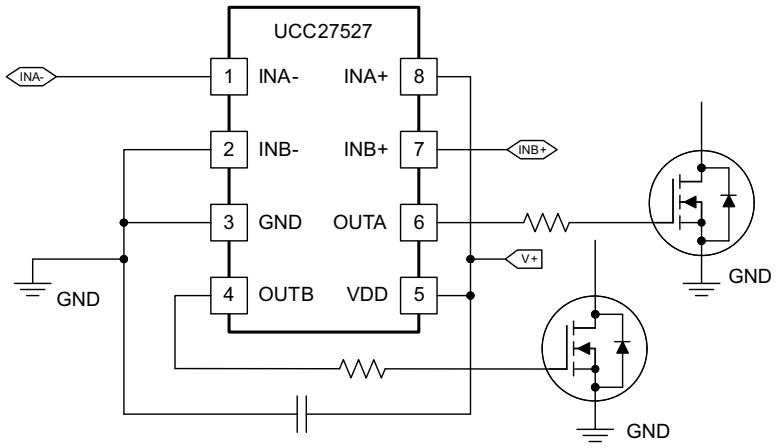

Figure 26. UCC27527 Channel A in Inverting and Channel B in Non-Inverting Configuration, (enable function not used)

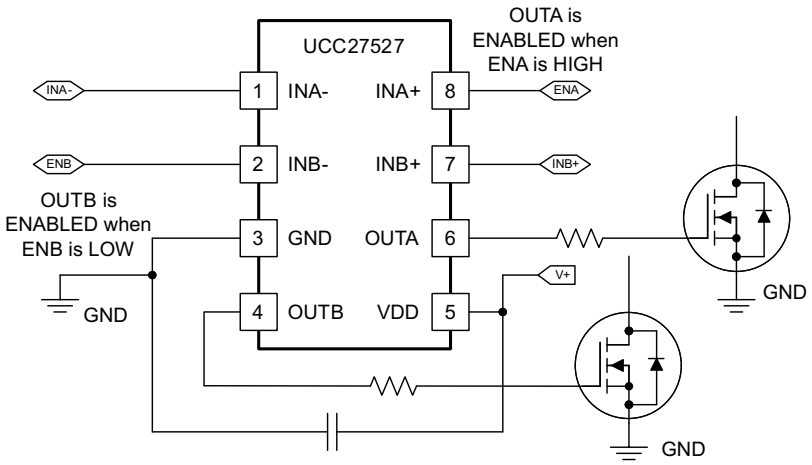

Figure 27. UCC27527 Channel A in Inverting and Channel B in Non-Inverting Configuration, (enable function implemented)

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Introduction

The UCC2752x family of products represent Texas Instruments' latest generation of dual-channel, low-side high-speed gate driver devices featuring 5-A source/sink current capability, industry best-in-class switching characteristics and a host of other features listed in table below all of which combine to guarantee efficient, robust and reliable operation in high-frequency switching power circuits.

Table 3. UCC27527 and UCC27528 Features and Benefits

FEATURE	BENEFIT
Best-in-class 13-ns (typ) propagation delay	Extremely low pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2x) current capability, ease of driving parallel power switches
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design
Expanded operating temperature range of -40°C to 140°C (See ELECTRICAL CHARACTERISTICS table)	
VDD UVLO Protection	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held Low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Outputs enabled when enable pins (ENx) in floating condition	Pin-to-pin compatibility with UCC2732X family of products from TI, in designs where pin #1, 8 are in floating condition
CMOS input threshold logic	Enhanced noise immunity, higher threshold level and wider hysteresis which is a function of VDD supply voltage and ability to employ RCD delay circuits on input pins.
Ability of input and enable pins to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture

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VDD and Under Voltage Lockout

The UCC2752x devices have internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs. The UVLO is typically 4.25 V with 350-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power-up, the UCC2752x driver-device output remains LOW until the V_{DD} voltage reaches the UVLO threshold if Enable pin is active or floating. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation in Figure 28 shows that the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. The inverting operation in Figure 29 shows that the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. With UCC27527 the output turns to high state only if INX+ is high and INX- is low after the UVLO threshold is reached.

Since the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

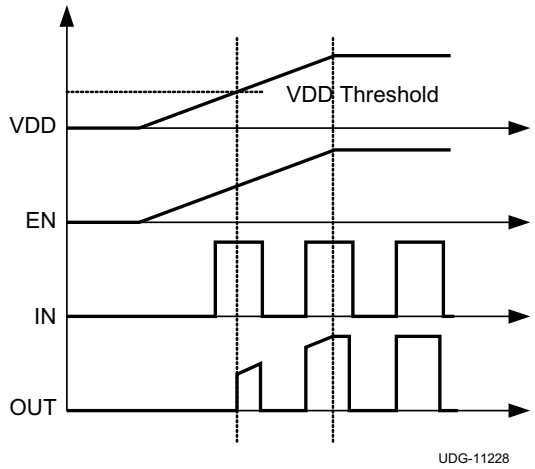

Figure 28. Power-Up Non-Inverting Driver

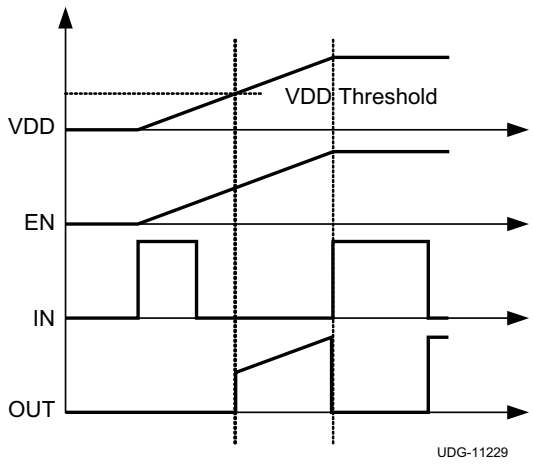

Figure 29. Power-Up Inverting Driver

Operating Supply Current

The UCC2752x products feature very low quiescent I_{DD} currents. The typical operating supply current in Under Voltage Lock-Out (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 8, Figure 9 and Figure 10. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 9) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the enable pins and inverting input pins. For example when the inverting Input pins are pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to Figure 6 though Figure 7). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load in both channels is provided in Figure 20. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

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Input Stage

The Input pins of UCC2752X gate driver devices are based on what is known as CMOS input threshold logic. In CMOS input threshold logic the threshold voltage level is a function of the bias voltage on the VDD pin of the device. The typical high threshold is 55% of VDD supply voltage and the typical low threshold is 38% of VDD supply voltage. There is built in hysteresis which is typically 17% of VDD supply voltage.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic will be higher (eg. VINH = 5.5 V if VDD = 10 V) than what is offered by the more common TTL and CMOS compatible input threshold logic where VINH is typically less than 3 V). The same is true of the input threshold hysteresis parameter as well. This offers the following benefits:

- Better noise immunity which is desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown below:

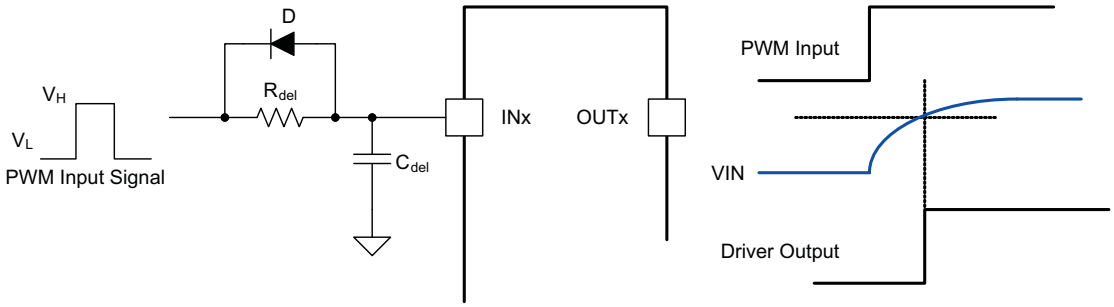

Figure 30. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln\left(\frac{V_L - V_{IN\_H}}{V_H - V_L} + 1\right) \quad (1)$$

The UCC2752x devices feature an important safety feature, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD pull-up resistors on all the inverting inputs (INA-, INB- in UCC27527) or GND pull-down resistors on all the non-inverting input pins (INA, INB in UCC27528 and INA+, INB+ in UCC27527), as shown in the device's block diagrams.

While UCC27528 features one input pin per channel, the UCC27527 features a dual input configuration with two input pins available to control the output state of each channel. With the UCC27527 device the user has the flexibility to drive each channel using either a non-inverting input pin (INx+) or an inverting input pin (INx-). The state of the output pin is dependent on the bias on both the INx+ and INx- pins (where x = A, B). Once an input pin has been chosen to drive a channel, the other input pin of that channel (the *unused* Input pin) must be properly biased in order to enable the output of the channel. The *unused* input pin cannot remain in a floating condition because, as mentioned earlier, whenever any input pin is left in a floating condition, the output of that channel is disabled using the internal pull-up and down resistors for safety purposes. Alternatively, the *unused* input pin can effectively be used to implement an enable and disable function, as explained below.

- In order to drive the channel “x” (x = A or B) in a non-inverting configuration, apply the PWM control input signal to INx+ pin. In this case, the *unused* input pin, INx-, must be biased low (eg. tied to GND) in order to enable the output of this channel.
  - Alternately, the INx- pin can be used to implement the enable and disable function using an external logic signal. OUTx is disabled when INx- is biased high and OUTx is enabled when INX- is biased low.
- In order to drive the channel “X” (X = A or B) in an inverting configuration, apply the PWM control input signal to INX- pin. In this case, the *unused* input pin, INX+, must be biased high (eg. tied to VDD) in order to enable the output of the channel.
  - Alternately, the INX+ pin can be used to implement the enable and disable function using an external logic signal. OUTX is disabled when INX+ is biased low and OUTX is enabled when INX+ is biased high.
- Finally, it is worth noting that the UCC27527 output pin can be driven into high state ONLY when INx+ pin is biased high AND INx- input is biased low.

Refer to the input and output logic truth table and typical application diagram for additional clarification.

Enable Function

The enable function is an extremely beneficial feature in gate driver devices especially for certain applications such as synchronous rectification where the driver outputs can be disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

UCC27528 device is provided with independent enable pins ENx for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active high operation). Thus when ENx pins are driven high the drivers are enabled and when ENx pins are driven low the drivers are disabled. Like the input pins, the enable pins are also based on a TTL/CMOS compatible input threshold logic that is independent of the supply voltage and can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC2752X devices also feature tight control of the Enable function threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 13). The ENx pins are internally pulled up to VDD using pull-up resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins can be left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this allows the UCC27528 device to be pin-to-pin compatible with TI's previous generation drivers UCC27323/4/5 respectively, where pins #1, 8 are N/C pins. If the channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together.

The UCC27527 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function can be easily implemented in UCC27527 using the unused input pin. When INx+ is pulled-down to GND or INx- is pulled-down to VDD, the output is disabled. Thus INx+ pin can be used like an enable pin that is based on active high logic, while INx- can be used like an enable pin that is based on active low logic. It is important to note that while the ENA, ENB pins in the UCC27528 are allowed to be in floating condition during standard operation and the outputs will be enabled, the INx+, INx- pins in UCC27527 are not allowed to be floating since this will disable the outputs.

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Output Stage

The UCC2752x device output stage features a unique architecture on the pull-up structure which delivers the highest peak Source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn-on. This is accomplished by briefly turning-on on the N-Channel MOSFET during a narrow instant when the output is changing state from Low to High.

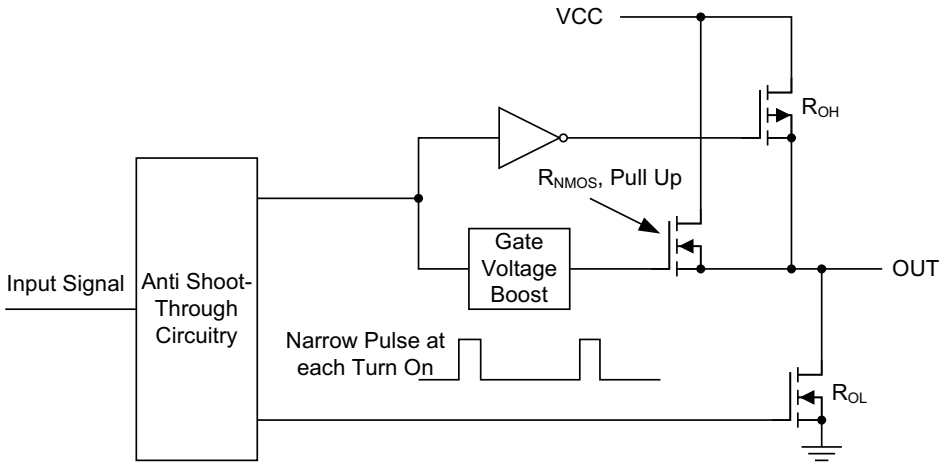

Figure 31. UCC2752X Gate Driver Output Structure

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Thus it should be noted that effective resistance of UCC2752x pull-up stage during turn-on instant is much lower than what is represented by R_{OH} parameter.

The pull-down structure in UCC2752x is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of the impedance of the pull-down stage in the device. In UCC2752x, the effective resistance of the hybrid pull-up structure during turn-on is estimated to be approximately 1.5 x R_{OL}, estimated based on design considerations.

Each output stage in UCC2752x is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low drop-out. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC2752x devices are particularly suited for dual-polarity, symmetrical drive gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is due to the extremely low drop-out offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

Low Propagation Delays and Tightly Matched Outputs

The UCC2752x driver devices offer a very low propagation delay of 17-ns (typical) between input and output which offers lowest level of pulse transmission distortion available in the industry for high-frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs can be driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typ) matched internal propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs may be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turn-on delay difference.

Since the CMOS input threshold of UCC27528 allows the use of slow dV/dt input signals, when paralleling outputs for obtaining higher peak output current capability, it is recommended to connect external gate resistors directly to the output pins to avoid shoot-through current conduction between the 2 channels, as shown in Figure 32. While the two channels are inherently very well matched (4-ns Max propagation delay), it should be noted that there may be differences in the input threshold voltage level between the two channels or differences in the input signals which can cause the delay between the two outputs.

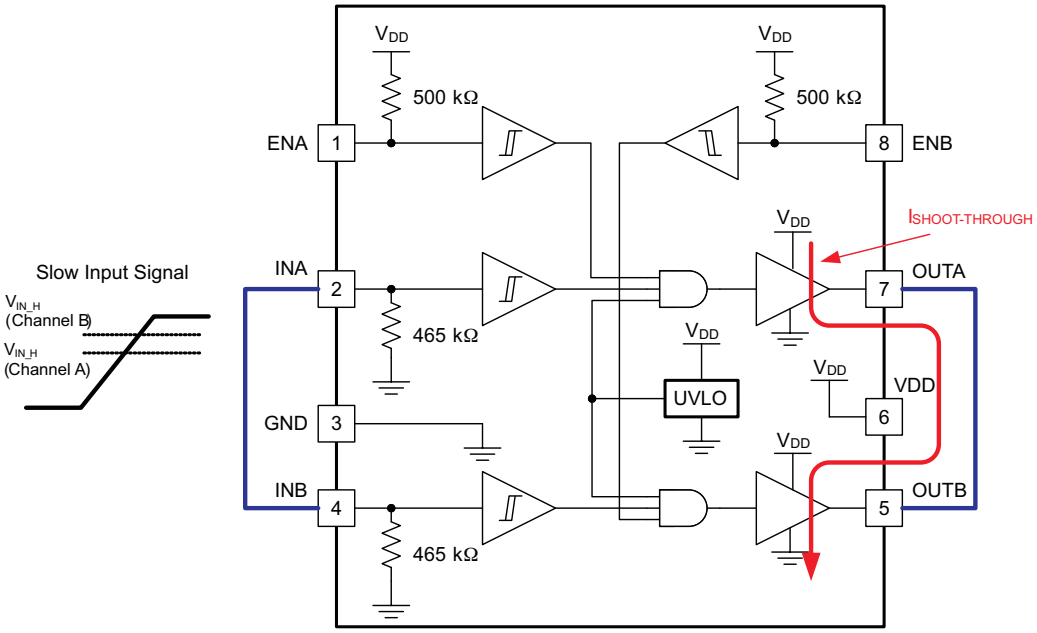

Figure 32. Slow Input Signal May Cause Shoot-Through Between Channels During Paralleling

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Drive Current and Power Dissipation

The UCC27527 and UCC27528 family of drivers are capable of delivering 5-A of current to a MOSFET gate for a period of several hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Since UCC2752x features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

where is load capacitor and is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{3}$$

where f_{SW} is the switching frequency.

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss can be calculated as:

$$P_G = 10\,\text{nF} \times 12\,\text{V}^2 \times 300\,\text{kHz} = 0.432\,\text{W} \tag{4}$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{LOAD}V_{DD}$ to provide the following equation for power:

$$P_G = C_{LOAD}V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (5)$$

Assuming that UCC2752x is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss can be calculated as:

$$P_G = 2 \times 60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \quad (6)$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET is being turned-on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \quad (7)$$

where $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 1.5 x R_{OL}.

In addition to the above gate charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pull-up and pull-down resistors), enable, and UVLO sections. Referring to the Figure 9 it can be seen that the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation can be simply calculated as:

$$P_Q = I_{DD}V_{DD} \quad (8)$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6\,mA \times 12\,V = 7.2\,mW \quad (9)$$

Clearly, this is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current can be estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (10)$$

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Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27527 and UCC27528 family of drivers is available in two different packages to cover a range of application requirements. The thermal metrics for each of these packages are summarized in the Thermal Information section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled, "IC Package Thermal Metrics" (Texas Instrument's Literature Number SPRA953A).

Among the different package options available in the UCC2752x family, of particular mention is the DSD package when it comes to power dissipation capability. The 3-mm x 3-mm WSON (DSD) package offer a means of removing the heat from the semiconductor junction through the exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the WSON-8 package is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate of the device which is the ground of the device. It is recommended to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

PCB Layout

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC27527 and UCC27528 family of gate drivers incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (5-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the Output pins and the Gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at 2 instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power MOSFET, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- In noisy environments, it may be necessary to tie inputs of an unused channel of UCC27527 to VDD (in case of INx+) or GND (in case of INX-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output.

PACKAGING INFORMATION

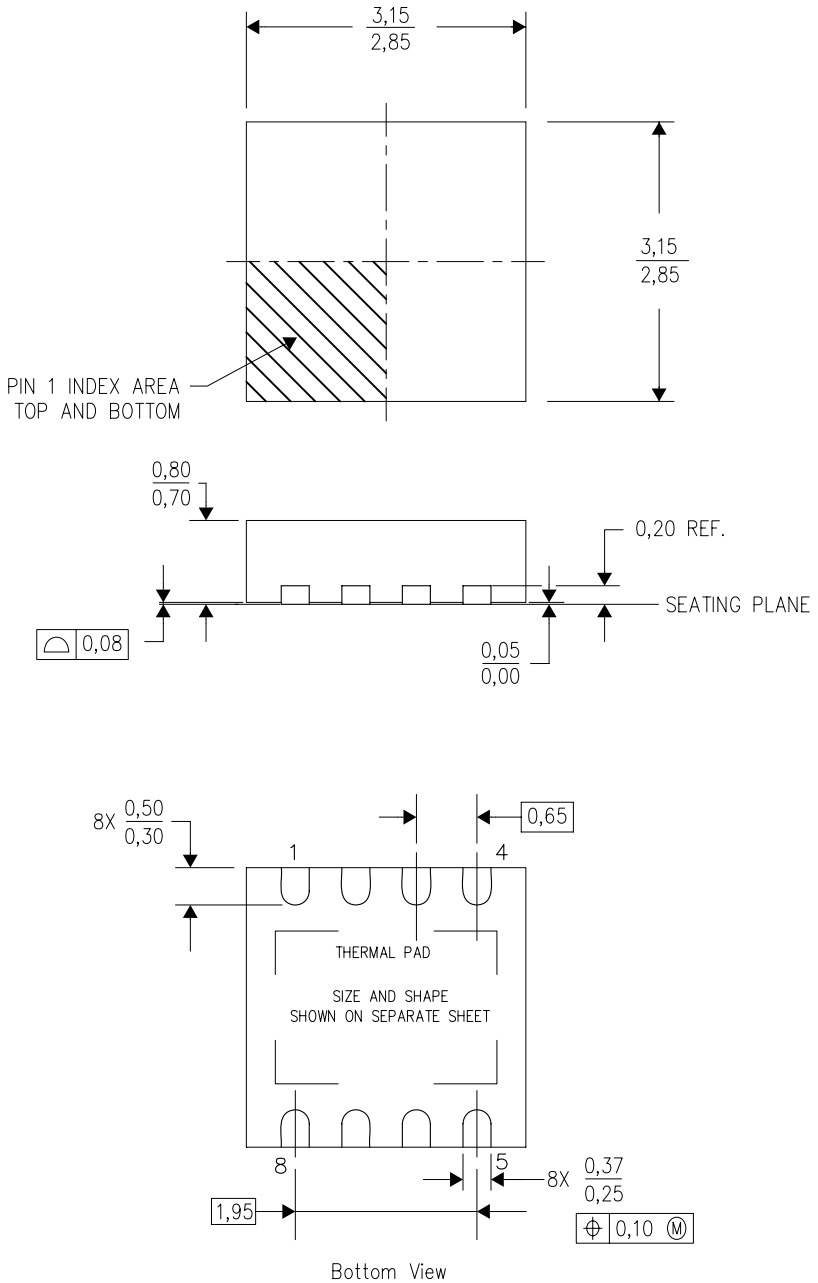
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC27528D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27528DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27528DSDR	PREVIEW	SON	DSD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC27528DSDT	PREVIEW	SON	DSD	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

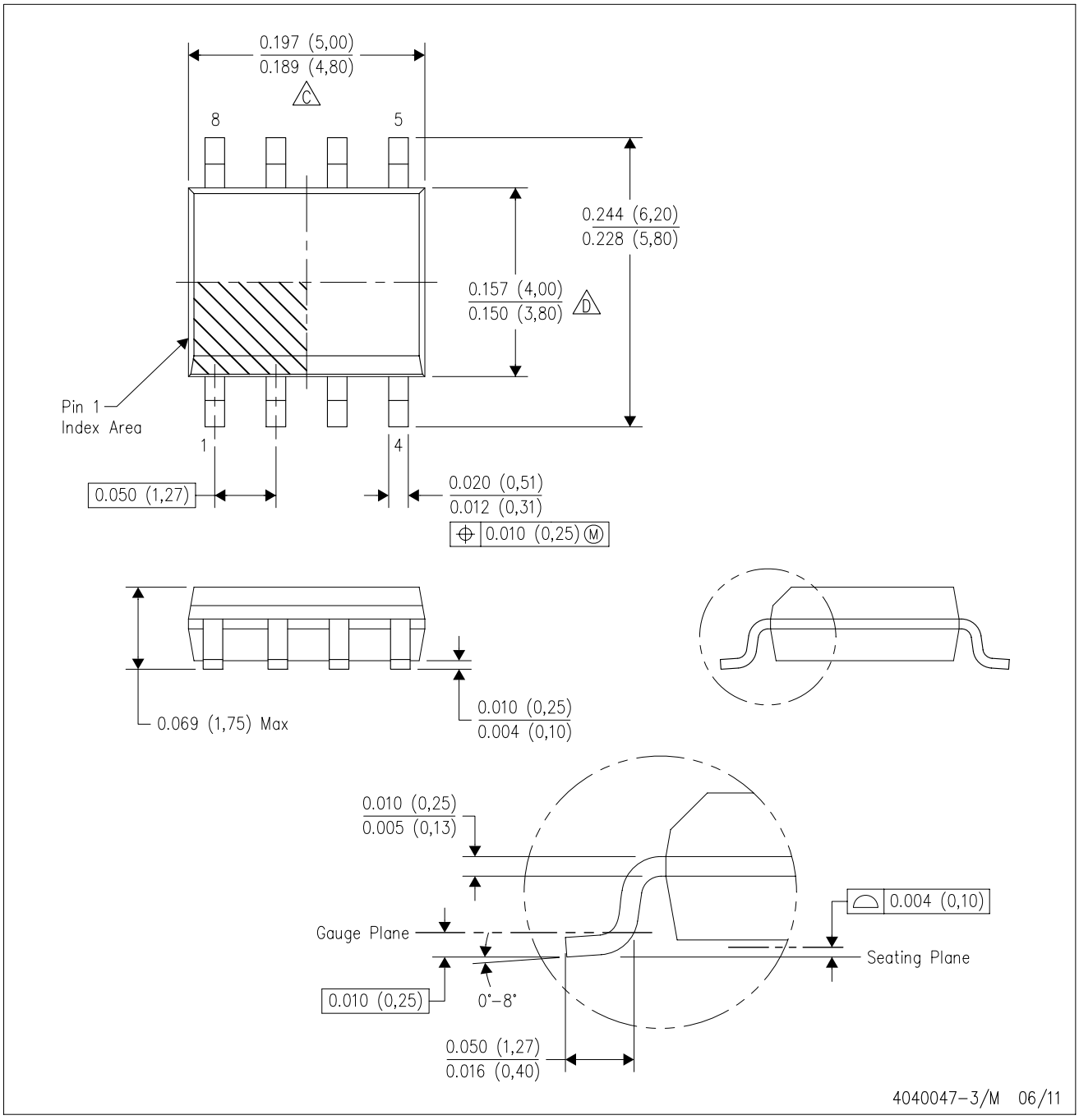
DSD (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4207382/B 01/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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